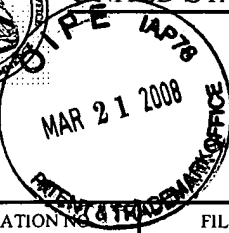




UNITED STATES PATENT AND TRADEMARK OFFICE

177

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov



APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/591,178

08/30/2006

Pierre Blanchard

4590-556

7764

33308 7590 03/14/2008
LOWE HAUPTMAN & BERNER, LLP
1700 DIAGONAL ROAD, SUITE 300
ALEXANDRIA, VA 22314

EXAMINER

GUMEDZOE, PENIEL M

ART UNIT PAPER NUMBER

2891

MAIL DATE DELIVERY MODE

03/14/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/591,178	BLANCHARD, PIERRE	
	Examiner	Art Unit	
	PENIEL M. GUMEDZOE	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 December 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Applicant's amendment filed on December 31, 2007 is acknowledged and papers submitted have been placed in the records.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Art Unit: 2815

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamimura et al. ('565) and further in view of Kub ('604).

Kamimura et al. ('565) disclose a method for fabricating a reading diode comprising: producing two electrodes separated by a gap above a substrate, said electrodes being a last electrode of a CCD shift register and a reset electrode for emptying electrical charges received by the reading diode from the shift register, forming an insulator layer over the electrodes and exposing the space between the two electrodes, depositing a layer of doped polycrystalline silicon in the space entering in contact with the substrate and selectively patterning the polycrystalline silicon, depositing an insulating layer above the polycrystalline silicon and locally etching an opening in the insulating layer outside the space lying between the electrodes, depositing and etching a metal to form a contact with the polycrystalline through the opening (see Fig. 1 and column 2 lines 26-63 of '565 and note that the last electrodes of the CCD register would have the same structure and configuration as the ones shown on Fig. 1 since the electrodes structure repeats a finite number of times). But Kamimura et al. ('565) do not appear to explicitly disclose thermally oxidizing the electrodes to form the electrodes insulating layer.

However Kub ('604) discloses oxidizing electrodes to form insulating layers (see Fig.2 and column 5 lines 55-68 of '604).

It would have been obvious to One of Ordinary Skill in the Art at the time the invention was made, to have formed polysilicon electrodes and oxidized them to form the insulating film 6 of the device of '565. One would have been motivated to do so because it is a simple and commonly known way of forming insulating layer on polycrystalline silicon (this is also admitted by applicant).

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamimura et al. ('565) and Kub ('604) and further in view of Zoroglu ('535).

Kamimura et al. ('565) and Kub ('604) disclose all the limitations of claim 1 as stated above but do not appear to explicitly disclose using nitride as insulating layer above the doped polysilicon, leaving uncovered and covered portions of the doped polysilicon layer and oxidizing the doped polysilicon layer until a silicon pattern is obtained which comprises only the covered zones.

However Zoroglu ('535) discloses oxidizing polysilicon layer having covered (with a passivation layer) and uncovered portions to form electrodes (see Figs. 6-9 and column 4 line 23 through column 5 lines 1-30 of '535).

It would have been obvious to One of Ordinary Skill in the Art at the time the invention was made, to have used silicon nitride as passivation layer and formed the doped polysilicon electrode according to the method of '535. One would have been motivated to do so because silicon nitride is a commonly used passivation layer for electrodes in Microfabrication and the oxidation step would have avoided the etching step for removing uncovered portions of the doped polysilicon electrode.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamimura et al. ('565), Kub ('604), Zoroglu ('535) and further in view of Wolf (Silicon Processing for the VLSI Era, page 331).

Kamimura et al. ('565), Kub ('604) and Zoroglu ('535) disclose all the limitations of claim 2 as stated above but do not appear to explicitly disclose chemically attacking the unprotected portions of the doped polysilicon in order to remove it as much as possible before to oxidation step.

However Wolf discloses partially etching unprotected portions of a silicon layer before oxidizing (see page 331 of Wolf).

It would have been obvious to One of Ordinary Skill in the Art at the time the invention was made, to have partially etched the unprotected portions of the doped polysilicon before oxidizing the polysilicon layer. One would have been motivated to do so because doing so would have allowed the oxidized portions to have planar surface with the protected portions (see the first paragraph on page 331 of Wolf).

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens ('990) and further in view of Kamimura et al. ('565).

Stevens disclosed an integrated circuit comprising a CCD register with a readout diode at the end of the register, between the last electrode of the register and a reset electrode for emptying electrical charges received by the reading diode, wherein the readout diode includes a doped region delimited on one side by the electrodes and on the other side by region of thick silicon oxide (see Figs. 1-4 and 6, column 2 lines 44

Art Unit: 2815

through column line 68, column 4 line 63 through column 5 line 2 of '990). But Stevens ('990) does not appear to explicitly disclose the doped region being entirely covered with a layer of polycrystalline silicon delimited according to a pattern which extends partly above the thick oxide (it rather teaches aluminum in column 4 lines 63-64), an insulating layer covering the silicon pattern and having an opening not located above the doped region, and a conductive layer above the insulating layer and in contact with the silicon layer through the opening.

However, Kamimura et al. ('565) disclose an insulating layer covering a doped polycrystalline silicon pattern and having an opening not located directly above the doped contact region, and a conductive layer above the insulating layer and in contact with the silicon layer through the opening (see Fig. 1 and column 2 lines 26-63 of '565).

It would have been obvious to One of Ordinary Skill in the Art at the time the invention was made, to have used doped polycrystalline (instead of aluminum), covered the polycrystalline silicon pattern and made an opening not located directly above the doped contact region, and to have formed a conductive layer above the insulating layer and in contact with the silicon layer through the opening. One would have been motivated to do so in order to provide interconnect contact for the diode and also because the doped polycrystalline is a functional equivalent of Aluminum.

The Examiner notes that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See, e.g.,

Art Unit: 2815

In re Pearson, 181 USPQ 641 (CCPA); *In re Minks*, 169 USPQ 120 (Bd Appeals); *In re Casey*, 152 USPQ 235 (CCPA 1967); *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

See MPEP §2114. The recitation of "for emptying electrical charges received by the reading diode" does not distinguish the present invention over the prior art of Kamimura et al. ('565) which teaches the structure as claimed.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens ('990), Kamimura et al. ('565) and further in view of Spangler et al. ('064).

Stevens ('990) and Kamimura et al. ('565) disclose all the limitations of claim 4 as stated above but do not appear to explicitly disclose the polycrystalline layer covered with silicon nitride having the same pattern as the polycrystalline silicon, itself covered by an insulating layer and both nitride and insulating film having an opening located at the same position.

However, Spangler et al. ('064) disclose using nitride layer to cover doped polysilicon to prevent diffusion of impurities (see layer 160 on Fig. 5 and column 12 lines 50-64 of '064).

It would have been obvious to One of Ordinary Skill in the Art at the time the invention was made, to have covered the doped polycrystalline silicon pattern (in the device as per claim 4 rejection) with a silicon nitride layer, itself covered by the insulating film 8 and made a hole through both layers to allow contact with conductive layer 9 (see Fig. 1 of '565 and column 2 lines 53-62). One would have been motivated

Art Unit: 2815

to do so to prevent impurities diffusion. Note that the nitride layer would have the same pattern as the polycrystalline silicon since the insulating layer it would replace as per claim 4 rejection above covers said polycrystalline according to the same pattern (see Fig. 1 of '565).

9. The prior art made of record and not relied upon are considered pertinent to applicant's disclosure.

Tsunai (US 2004/0109075) and Nagakawa et al. (US 5,416,346) teach forming CCD image sensors.

Response to Arguments

10. Applicant's arguments filed on December 31, 2007 have been fully considered but they are not persuasive.

The recitation of "reading" and "said electrodes being last electrode ... reset electrode for emptying ... the shift register" in claim 1 has not been given patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *Kropa v. Robie*, 88 USPQ 478 (CCPA 1951).

Applicant's argument that one of ordinary skill in the art would not have provided insulating layer 6 as a thermal insulation is not convincing. Kub ('604) does teach providing such insulation between polysilicon structures as stated in claim 1 rejection

Art Unit: 2815

above and this shows that the polysilicon structures would not have completely disappeared as Applicant further argues. Kub ('604) discloses the contact 44 being aluminum (see col. 6 line 9 of '604) and this may explain why a thermal oxidation would not have been appropriate to create a thermal insulation layer above it. If it was made of polysilicon, an ordinary skill in the art would have obviously insulated it by thermal oxidation as for the other polysilicon structures surrounding it.

Applicant's argument in regard to claim 4 rejection is not convincing. Examiner believes that since Kamimura ('565) teaches fabricating a CCD device including a diode and an insulating film to protect a contact running from said diode and the complete device, it is a relevant teaching reference for making the same protective insulating structure for the CCD device of Stevens ('990) whether or not the said diode is a reading diode.

Re applicant's argument, and this, wherever stated in Applicant's arguments, that the references cited or motivations to combine put forward by the Examiner are not relevant to the problem that Applicant is trying to solve (reducing a diode size), Examiner points out that the motivations to combine (as stated in claims 1-5 rejections above) are proper for one of ordinary skill in the art and do not require the goal or motivation to solve the same problem as Applicant in order to be valid.

Re applicant's argument that silicon nitride is not suggested in the configuration which is defined in claim 4, Examiner points out that the motivation to use silicon nitride to protect the doped polycrystalline was stated in claim 5 rejection.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peniel M. Gumedzoe whose telephone number is 571-270-3041. The examiner can normally be reached on M-F from 9:30 AM to 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister, can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For

Art Unit: 2815

more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

February 27, 2008

Peniel Gumedzoe

Examiner / Art Unit 2891

/Eugene Lee/

Primary Examiner, Art Unit 2815

Notice of References Cited	Application/Control No. 10/591,178		Applicant(s)/Patent Under Reexamination BLANCHARD, PIERRE	
	Examiner PENIEL M. GUMEDZOE		Art Unit 2891	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,416,346 A	05-1995	Nagakawa et al.	257/239
*	B	US-2004/0109075 A1	06-2004	Tsunai, Shiro	348/311
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.